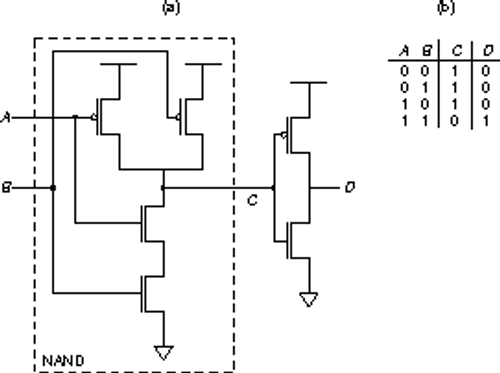
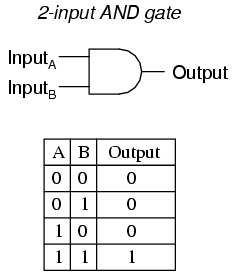
**Circuit Diagram & Truth Table:**

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**Code:**

* **Design Module**

module andgate(out,a,b);

input a,b;

output out;

wire x,y;

supply1 vdd;

supply0 gnd;

pmos p1(y,vdd,a);

pmos p2(y,vdd,b);

pmos p3(out,vdd,y);

nmos n1(x,gnd,a);

nmos n2(y,x,b);

nmos n3(out,gnd,y);

endmodule

* **TestBench**

module Baig;

reg a,b;

wire out;

andgate ng(out,a,b);

initial

begin

a=1'b0;b=1'b0;

#10

a=1'b0;b=1'b1;

#10

a=1'b1;b=1'b0;

#10

a=1'b1;b=1'b1;

#10

$finish;

end

endmodule